1. A method of forming shallow trench isolation regions in the manufacture of an integrated circuit device comprising:

depositing an etch stop layer on the surface of a semiconductor substrate;

etching a plurality of isolation trenches through said etch stop layer into said semiconductor substrate whereby narrow active areas and wide active areas of said semiconductor substrate are left between said isolation trenches;

depositing an oxide layer over said etch stop layer and within said isolation trenches using a high density plasma chemical vapor deposition process (HDP-CVD) having a deposition component and a sputtering component wherein after said oxide layer fills said isolation trenches, said deposition component is discontinued while continuing said sputtering component until said oxide layer is at a desired depth in said isolation trenches whereby said oxide layer within said isolation trenches is disconnected from said oxide layer overlying said etch stop layer;

thereafter etching away said oxide layer overlying said etch stop layer in said wide active areas wherein oxide layer residues are left overlying said etch stop layer; and

removing said etch stop layer and said oxide residues to complete planarized said shallow trench isolation regions in said manufacture of said integrated circuit device.

2. The method according to Claim 1 further comprising growing a pad oxide layer on said semiconductor substrate before said step of depositing said etch stop layer.

3. The method according to Claim 1 wherein said etch stop layer comprises silicon nitride and is deposited by chemical vapor deposition to a thickness of between about 1500 and 2500 Angstroms.

4. The method according to Claim 1 further comprising growing a liner layer within said isolation trenches before said step of depositing said oxide layer within said isolation trenches.

5. The method according to Claim 1 wherein said step of removing said etch stop layer and said oxide residues comprises a hot phosphoric acid (H_3PO_4) dip.

6. The method according to Claim 1 wherein said step of removing said etch stop layer and said oxide residues comprises:

etching away said oxide residues using an etching recipe selective to oxide with respect to said etch stop layer; and

thereafter removing said etch stop layer using a hot phosphoric acid (H_3PO_4) dip.

7. The method according to Claim 1 further comprising fabricating semiconductor device structures in and on said semiconductor substrate between said isolation trenches.

8. A method of forming shallow trench isolation regions in the manufacture of an integrated circuit device comprising:

growing a pad oxide layer on the surface of a semiconductor substrate;

depositing a first etch stop layer overlying said pad oxide layer;

etching a plurality of isolation trenches through said first etch stop layer and said pad oxide layer into said semiconductor substrate whereby narrow active areas and wide active areas of said semiconductor substrate

are left between said isolation trenches;

depositing an oxide layer over said first etch stop layer and within said isolation trenches using a high density plasma chemical vapor deposition process (HDP-CVD) having a deposition component and a sputtering component wherein after said oxide layer fills said isolation trenches, said deposition component is discontinued while continuing said sputtering component until said oxide layer is sputtered back within said isolation trenches to the level of said pad oxide layer;

depositing a second etch stop layer over said oxide layer using a high density plasma chemical vapor deposition process (HDP-CVD) having a deposition component and a sputtering component whereby said second etch stop layer is sputtered away overlying said oxide layer overlying said first etch stop layer in said narrow active areas and whereby said second etch stop layer remains overlying said oxide layer overlying said first etch stop layer in said wide active areas;

thereafter etching away said second etch stop layer overlying said oxide layer in said wide active areas;

thereafter etching away said oxide layer overlying said first etch stop layer in said narrow and said wide active areas; and

removing said first and second etch stop layers to

complete planarized said shallow trench isolation regions in said manufacture of said integrated circuit device.

9. The method according to Claim 8 wherein said first etch stop layer comprises silicon nitride and is deposited by chemical vapor deposition to a thickness of between about 1500 and 2500 Angstroms.

10. The method according to Claim 8 further comprising growing a liner layer within said isolation trenches before said step of depositing said oxide layer within said isolation trenches.

11. The method according to Claim 8 wherein said step of depositing said oxide layer by HDP-CVD has a deposition to sputter ratio of about 3.6.

12. The method according to Claim 8 wherein said step of depositing said second etch stop layer by HDP-CVD has a deposition to sputter ratio of about 2.

13. The method according to Claim 8 wherein said second etch stop layer comprises silicon nitride having a thickness of between about 500 and 2000 Angstroms.

14. The method according to Claim 8 wherein said step of removing said first and second etch stop layers comprises a hot phosphoric acid (H_3PO_4) dip.

15. The method according to Claim 8 further comprising fabricating semiconductor device structures in and on said semiconductor substrate between said isolation trenches.

16. A method of forming shallow trench isolation regions whereby a polishing process is not used in the manufacture of an integrated circuit device comprising:

depositing an etch stop layer on the surface of a semiconductor substrate;

etching a plurality of isolation trenches through said etch stop layer into said semiconductor substrate whereby narrow active areas and wide active areas of said semiconductor substrate are left between said isolation trenches;

depositing an oxide layer over said etch stop layer and within said isolation trenches using a high density plasma chemical vapor deposition process (HDP-CVD) having a deposition component and a sputtering component wherein after said oxide layer fills said isolation trenches, said deposition component is discontinued

while continuing said sputtering component until said oxide layer is at a desired depth in said isolation trenches whereby said oxide layer within said isolation trenches is disconnected from said oxide layer overlying said etch stop layer;

thereafter etching away said oxide layer overlying said etch stop layer in said wide active areas wherein oxide layer residues are left overlying said etch stop layer; and

removing said etch stop layer and said oxide residues without using a polishing process to complete planarized said shallow trench isolation regions in said manufacture of said integrated circuit device.

17. The method according to Claim 16 further comprising growing a pad oxide layer on said semiconductor substrate before said step of depositing said etch stop layer.

18. The method according to Claim 16 wherein said etch stop layer comprises silicon nitride and is deposited by chemical vapor deposition to a thickness of between about 1500 and 2500 Angstroms.

19. The method according to Claim 16 further comprising growing a liner layer within said isolation trenches before said step of depositing said oxide layer within said isolation trenches.

20. The method according to Claim 16 wherein said step of removing said etch stop layer and said oxide residues comprises a hot phosphoric acid (H_3PO_4) dip.

21. The method according to Claim 16 wherein said step of removing said etch stop layer and said oxide residues comprises:

etching away said oxide residues using an etching recipe selective to oxide with respect to said etch stop layer; and

thereafter removing said etch stop layer using a hot phosphoric acid (H_3PO_4) dip.

22. The method according to Claim 16 further comprising fabricating semiconductor device structures in and on said semiconductor substrate between said isolation trenches.

23. A method of forming shallow trench isolation regions whereby a polishing process is not used in the

manufacture of an integrated circuit device comprising:

growing a pad oxide layer on the surface of a semiconductor substrate;

depositing a first etch stop layer overlying said pad oxide layer;

etching a plurality of isolation trenches through said first etch stop layer and said pad oxide layer into said semiconductor substrate whereby narrow active areas and wide active areas of said semiconductor substrate are left between said isolation trenches;

depositing an oxide layer over said first etch stop layer and within said isolation trenches using a high density plasma chemical vapor deposition process (HDP-CVD) having a deposition component and a sputtering component wherein after said oxide layer fills said isolation trenches, said deposition component is discontinued while continuing said sputtering component until said oxide layer is sputtered back within said isolation trenches to the level of said pad oxide layer;

depositing a second etch stop layer over said oxide layer using a high density plasma chemical vapor deposition process (HDP-CVD) having a deposition component and a sputtering component whereby said second etch stop layer is sputtered away overlying said oxide layer overlying said first etch stop layer in said

narrow active areas and whereby said second etch stop layer remains overlying said oxide layer overlying said first etch stop layer in said wide active areas;

thereafter etching away said second etch stop layer overlying said oxide layer in said wide active areas;

thereafter etching away said oxide layer overlying said first etch stop layer in said narrow and said wide active areas; and

removing said first and second etch stop layers without using a polishing process to complete planarized said shallow trench isolation regions in said manufacture of said integrated circuit device.

24. The method according to Claim 23 further comprising growing a liner layer within said isolation trenches before said step of depositing said oxide layer within said isolation trenches.

25. The method according to Claim 23 wherein said step of removing said first and second etch stop layers comprises a hot phosphoric acid (H_3PO_4) dip.